REMARKS

Claims 1-36 are pending in the Application. Claims 1-36 are rejected under 35 U.S.C. § 102(e). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

Applicants thank the Examiner for discussing the present Office Action and in particular the Lavelle et al. (U.S. Patent No. 6,020,901) reference in relation to claim 1 with Applicants on December 3, 2003.

I. REJECTIONS UNDER 35 U.S.C. § 102(e):

The Examiner has rejected claims 1-36 under 35 U.S.C. § 102(e) as being anticipated by Lavelle et al. (U.S. Patent No. 6,020,901) (hereinafter "Lavelle"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. § 102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

Applicants respectfully assert that Lavelle does not disclose "providing a user with a selectable option to allocate said memory space as a double buffered stereo or a single buffered stereo" as recited in claim 1 and similarly in claims 6, 11, 16, 23 and 30. The Examiner does not cite a passage that discloses the above-cited claim limitation. Instead, the Examiner cites passages that allegedly disclose one or more of the elements in the above-cited claim limitation. It is noted that a claimed invention is not a set of disembodied elements. The claimed invention as a whole must be considered in an anticipation rejection. M.P.E.P. § 2131.

The Examiner cites column 5, lines 27-23 and column 3, lines 42-44 of Lavelle as disclosing providing a user with a selectable option. Paper No. 3, page 2. Applicants respectfully traverse and assert that Lavelle instead discloses a rendering unit, rendering unit 610, that provides integer rendering as well as discloses PROM unit 540 that is a memory used to initialize fast frame buffer system 500 when the host workstation and computer system is powered on. Applicants respectfully assert that column 5, lines 27-23 and column 3, lines 42-44 of Lavelle has no relevance to providing a user with a selectable option. Further, Applicants respectfully assert that column 5, lines 27-23 and column 3, lines 42-44 of Lavelle has no relevance to providing a user with a selectable option to allocate the memory space as a double buffered stereo or a single buffered stereo. Applicants respectfully assert that the Examiner must clearly explain the above-cited passages with respect to the above-cited claim limitation, pursuant to 37 C.F.R. § 1.104(c)(2).

The Examiner further cites column 4, lines 18-29 of Lavelle as disclosing allocating the memory space as a double buffered stereo or a single buffered stereo. Paper No. 3, pages 2-3. Applicants respectfully traverse and assert that Lavelle instead discloses a doubled-buffered configuration as illustrated in Figure 4 as well as a single buffered configuration as illustrated in Figure 3. However, this passage does not disclose allocating a memory space as a double buffer stereo or a single buffered stereo. Further, this passage does not disclose providing a user with a selectable option to allocate a memory space as a double buffered stereo or a single buffered stereo. Thus, Lavelle does not disclose all of the limitations of claims 1, 6, 11, 16, 23 and 30, and thus Lavelle does not anticipate claims 1, 6, 11, 16, 23 and 30. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "allocating said memory space as one of said double buffered stereo and said single buffered stereo in response to said selectable option" as recited in claim 1 and similarly in claims 6, 11, 16, 23 and 30. The Examiner cites column 7, line 33 through column 8, line 34 of

Lavelle as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and asset that Lavelle instead discloses a bi-directional signal, as indicated by FIELD, that is an input signal when the timing generator, timing generator 580, is operated in slave mode. Applicants respectfully assert that the cited passage has no relevance with respect to the above-cited claim limitation. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passage with respect to the above-cited claim limitation, pursuant to 37 C.F.R. § 1.104(c)(2). Thus, Lavelle does not disclose all of the limitations of claims 1, 6, 11, 16, 23 and 30, and thus Lavelle does not anticipate claims 1, 6, 11, 16, 23 and 30. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "reading a command line option to determine allocation of a memory space" as recited in claim 16 and similarly in claims 23 and 30. The Examiner cites column 2, lines 43-52 of Lavelle as discussing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and asset that Lavelle instead discloses a control unit of a fast frame buffer controller that includes a command unit as well as a video refresh control unit. Applicants respectfully assert that there is no relevancy of the cited passage with respect to reading a command line option to determine allocation of a memory space. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passage with respect to reading a command line option to determine allocation of a memory space pursuant to 37 C.F.R. § 1.104(c)(2). Thus, Lavelle does not disclose all the limitations of claim 16, 23 and 30, and thus Lavelle does not anticipate claim 16, 23 and 30. M.P.E.P § 2131.

Claims 2-5, 7-10, 12-15, 17-22, 24-29 and 31-36 each recite combinations of features including the above combinations, and thus are not anticipated for at least the above stated reasons. Claims 2-5, 7-10, 12-15, 17-22, 24-29 and 31-36 recite additional features, which, in combination with the features of the claims upon which they depend are not anticipated by Lavelle.

For example, Lavelle does not disclose "wherein if said memory space is allocated for said single buffered stereo then a greater portion of said memory space is available for at least one of texture memory and off-screen cache" as recited in claim 2 and similarly in claims 7, 12, 17, 24 and 31. The Examiner cites column 1, line 19; column 5, lines 6-14; and column 6, lines 11-30 of Lavelle as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Lavelle instead discloses using texture maps when rendering detailed surface geometry. While Lavelle discloses using texture maps, Lavelle does not disclose that if a memory space is allocated for single buffered stereo then a greater portion of that memory space is available for texture memory or off-screen cache. Thus, Lavelle does not disclose all of the limitations of claim 2, 7, 12, 17, 24 and 31, and thus Lavelle does not anticipate claims 2, 7, 12, 17, 24 and 31. M.P.E.P. §2131.

Applicants further assert that Lavelle does not disclose "setting a flag to indicate that said memory space is allocated for said single buffered stereo" as recited in claim 3 and similarly in claims 8, 13, 18, 25 and 32. The Examiner cites column 7, lines 7, line 33 through column 8, line 34 of Lavelle as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and assert that Lavelle instead discloses a bi-directional signal that is an input signal when the timing generator, timing generator 580, is operated in slave mode. Applicants respectfully assert that there is no relevance of the cited passage with respect to setting a flag to indicate that a memory space is allocated for a single buffered stereo. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passage with respect to setting the flag to indicate that a memory space is allocated for a single buffered stereo, pursuant to 37 C.F.R. § 1.104(c)(2). Thus, Lavelle does not disclose all of the limitations of claims 3, 8, 13, 18, 25 and 32, and thus Lavelle does not anticipate claims 3, 8, 13, 18, 25 and 32. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "setting a flag to indicate that said memory space is allocated for said double buffered stereo" as

recited in claim 4 and similarly in claims 9, 14, 19, 26 and 33. The Examiner cites column 7, line 33 through column 8, line 34 of Lavelle as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and assert that Lavelle instead discloses a bi-directional signal that is an input signal when a timing generator, timing generator 580, is operated in slave mode. Applicants respectfully assert that there is no relevancy of the cited passage with respect to setting a flag to indicate that a memory space is allocated for a double buffered stereo. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passage with respect to setting a flag to indicate that a memory space is allocated for a double buffered stereo, pursuant to 37 C.F.R. § 1.104(c)(2). Thus, Lavelle does not disclose all of the limitations of claims 4, 9, 14, 19, 26 and 33, and thus Lavelle does not anticipate claims 4, 9, 14, 19, 26 and 33. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "receiving said selectable option" as recited in claim 5 and similarly in claims 10, 15, 20, 27 and 37. The Examiner cites column 5, lines 1-6 and 27-33 of Lavelle as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and assert that Lavelle instead discloses an interface unit, interface unit 600, that is responsible for synchronizing data and requesting access clock domains. Further, Lavelle discloses a pipeline rendering unit, rendering unit 610, that provides integer rendering. Applicants respectfully assert that there is no relevancy of the cited passages with respect to receiving a selectable option to allocate a memory space as a double buffered stereo or a single buffered stereo. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passages with respect to the above-cited claim limitation, pursuant to 37 C.F.R. § 1.104(c)(2). Thus, Lavelle does not disclose all the limitations of claims 5, 10, 15, 20, 27 and 34, and thus Lavelle does not anticipate claims 5, 10, 15, 20, 27 and 34. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "reading said selectable option" as recited in claim 5 and similarly in claims 10, 15, 20, 27 and 34.

The Examiner cites column 5, lines 26 and 27-33 as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and assert that Lavelle instead discloses an interface unit, interface unit 600, that is responsible for synchronizing data and requesting access clock domains. Lavelle further discloses a pipeline rendering unit, rendering unit 610, that provides integer rendering. Applicants respectfully assert that there is no relevancy of the cited passages with respect to reading a selectable option to allocate a memory space as a double buffered stereo or a single buffered stereo. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passages with respect to the above-cited claim limitation, pursuant to 37 C.F.R. § 1.104(c)(2). Thus, Lavelle does not disclose all the limitations of claims 5, 10, 15, 20, 27 and 34, and thus Lavelle does not anticipate claims 5, 10, 15, 20, 27 and 34. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "determining whether to allocate said memory space as said double buffered stereo or said single buffered stereo in response to said reading step" as recited in claim 5 and similarly in claims 10, 15, 20, 27 and 37. The Examiner cites column 7, line 33 through column 8, line 34 of Lavelle as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Lavelle instead discloses a bi-directional signal that is an input signal when a timing generator, timing generator 580, is operated in slave mode. Applicants respectfully assert that there is no relevancy of the cited passage with respect to determining whether to allocate a memory space as a double buffered stereo or a single buffered stereo in response to reading a selectable option. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passage with respect to determining whether to allocate a memory space as a double buffered stereo or a single buffered stereo in response to reading a selectable option pursuant to 37 C.F.R. § 1.04(c)(2). Thus, Lavelle does not disclose all of the limitations of claims 5, 10, 15, 20, 27, 34, and thus Lavelle does not anticipate claims 5, 10, 15, 20, 27 and 34. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "reading a file storing a set of startup options, wherein one of said startup options comprises a default value overrideable by said command line option" as recited in claim 18 and similarly in claims 25 and 32. The Examiner cites column 5, lines 7-25 as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and assert that Lavelle instead discloses that the data flow between interface unit 600 and pixel data multiplexor 620 can occur using one of two parallel paths, either a bilateral direct path or a unilateral accelerated path via pipeline rendering unit 610. Applicants respectfully assert that there is no relevancy of the cited passage with respect to reading a file storing a set of startup options where one of the startup options comprises a default value overrideable by a command line option. Applicants respectfully assert that the Examiner must clearly explain the relevancy of the cited passage with respect to the above-cited claim limitation pursuant to 37 C.F.R. § 1.104(c)(2). Thus, Lavelle does not disclose all of the limitations of claims 18, 25 and 32, and thus Lavelle does not anticipate claims 18, 25 and 32. M.P.E.P § 2131.

Applicants further assert that Lavelle does not disclose "wherein said default value corresponds to allocating said memory space as said double buffered stereo" as recited in claim 19 and similarly in claims 26 and 33. The Examiner has not cited any passage within Lavelle as allegedly disclosing the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must cite a prior art reference that discloses each and every claim limitation. M.P.E.P. §2131. Thus, Lavelle does not disclose all the limitations of claims 19, 26 and 33, and thus Lavelle does not anticipate claims 19, 26 and 33. M.P.E.P. § 2131.

Applicants further assert that Lavelle does not disclose "wherein said command line option has a value corresponding to allocating said memory space as said single buffered stereo" as recited in claim 20 and similarly in claims 27 and 34. The Examiner has not cited any passage within Lavelle as allegedly disclosing the

above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must cite a prior art reference that discloses each and every claim limitation. M.P.E.P. §2131. Thus, Lavelle does not disclose all the limitations of claims 20, 27 and 34, and thus Lavelle does not anticipate claims 20, 27 and 34. M.P.E.P. § 2131.

Applicants further assert that Lavelle does not disclose "wherein said default value corresponds to allocating said memory space as said single buffered stereo" as recited in claim 21 and similarly in claims 28 and 35. The Examiner has not cited any passage within Lavelle as allegedly disclosing the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must cite a prior art reference that discloses each and every claim limitation. M.P.E.P. §2131. Thus, Lavelle does not disclose all the limitations of claims 21, 28 and 35, and thus Lavelle does not anticipate claims 21, 28 and 35. M.P.E.P. § 2131.

Applicants further assert that Lavelle does not disclose "wherein said command line option has a value corresponding to allocating said memory space as said double buffered stereo" as recited in claim 22 and similarly in claims 29 and 36. The Examiner has not cited any passage within Lavelle as allegedly disclosing the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must cite a prior art reference that discloses each and every claim limitation. M.P.E.P. §2131. Thus, Lavelle does not disclose all the limitations of claims 23, 30 and 36, and thus Lavelle does not anticipate claims 23, 30 and 36. M.P.E.P. § 2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within the cited prior art reference, and thus claims 1-36 are not anticipated by Lavelle.

II. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-36 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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